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WIDE FREQUENCY OFFSET CORRECTION USING ENCODED INTERBURST PHASE DIFFERENCES

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WIDE FREQUENCY OFFSET CORRECTION USING ENCODED INTERBURST PHASE DIFFERENCES

STATEMENT OF RELATED APPLICATIONS

The present application is related to the subject matter of the following four U.S. Patent Applications:

U.S. Patent App. No. 09/245,168, filed on February 5, 1999, entitled SYNCHRONIZATION IN OFDM SYSTEMS.

now US patent 6549592

U.S. Patent App. No. 09/244,754, filed on February 5, 1999, entitled ENHANCED SYNCHRONIZATION BURST FOR OFDM SYSTEMS.

U.S. Patent App. No. 09/469,715, filed on December 21, 1999, entitled WIDE RANGE FREQUENCY OFFSET ESTIMATION IN OFDM SYSTEMS.

U.S. Patent App. No. 09/415,014, filed on October 7, 1999, entitled TRANSMISSION OF SYSTEM CONFIGURATION INFORMATION.

These related patent applications are incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

The present invention relates to digital communications and more particularly to synchronization of frequency between a receiver and a transmitter.

In an OFDM (Orthogonal Frequency Division Multiplexing) communication system, a channel to be used for communication is divided into subchannels that are orthogonal to one another in the frequency domain. Data is communicated in a series of time domain bursts. To form each time domain burst an IFFT is applied to a group of frequency domain symbols and a cyclic prefix is added to the transform result prior to transmission. Transmission may involve conversion of the transform result to an analog signal, conversion of the analog signal to an intermediate frequency (IF), then upconversion to a desired selectable carrier frequency prior to final amplification and propagation across a transmission medium. Upconversion is typically achieved by mixing the IF signal with a variable frequency oscillator signal. The carrier frequency is varied by varying the oscillator frequency.

On the receiver end, preamplification is followed by downconversion to IF from the carrier frequency, again by mixing with the output of a variable frequency oscillator. The resulting IF signal is typically converted to a baseband digital symbol sequence. The cyclic prefix is removed and an FFT is applied to recover the original frequency domain symbols.

For successful communication, the transmitter and receiver should have a precise shared understanding of the transmission frequency. In the exemplary system described above, this means that the variable frequency oscillators of the transmitter and receiver should be locked to each other. Imprecision with respect to the transmission frequency will cause inaccurate recovery of the OFDM symbols. To maintain system performance, it is desirable to always maintain frequency offset between a transmitter and a receiver to within 1% of the spectral width occupied by a single frequency domain OFDM symbol.

When the receiver initially acquires the transmitter frequency, it is desirable that the synchronization system tolerates and corrects as wide as possible a frequency offset between the transmitter and receiver oscillators. This allows the use of much lower cost analog components for the receiver oscillator.

U.S. Patent App. No. 09/245,168, filed on February 5, 1999, and entitled SYNCHRONIZATION IN OFDM SYSTEMS discloses various systems and methods for synchronizing the receiver frequency of an OFDM receiver to the transmission frequency of an OFDM transmitter. One such system provides a supplemental cyclic prefix that follows the cyclic prefix used to orthogonalize the frequency domain subchannels. At the receiver end, this supplemental cyclic prefix is correlated to the corresponding time domain symbols within the principle portion of the time domain burst in order to compute a fine frequency offset, that is a fractional component of the frequency offset as measured in OFDM frequency domain symbol widths. Once the fine offset is computed, it may be corrected by use of appropriate control signals to the receiver variable frequency oscillator. This procedure corrects for frequency offsets that are a fraction of a frequency domain symbol width but after this correction the received frequency may still be offset from the transmit frequency by an integer number of frequency domain symbol widths.

The procedure for correction of this integer frequency offset takes advantage of frequency domain structure within each OFDM burst. Each OFDM burst includes regularly spaced training symbols having known predetermined values. The training symbols facilitate estimation of the channel response at the receiver and correction of the integer frequency offset. The integer frequency offset is corrected by finding the

frequency alignment that causes the received symbol values at the known training positions to correlate strongly between successive bursts.

It will be appreciated, however, that there is a limit to the acquisition range for this integer frequency offset correction technique. If the frequency offset is greater than the spacing between training symbols, then this offset correction technique may lock to a false alignment that differs from the correct alignment by an integer multiple of the training symbol spacing. The acquisition range is thus $\pm\frac{N}{2\upsilon}$ tones where N is the number of frequency domain symbols in a single OFDM burst and ν is the number of frequency domain symbols reserved for training.

Consider a millimeter wave application where the operating frequency is 28 GHz and where use of low cost analog components may cause an initial frequency offset of 10 parts per million (ppm) or 280 KHz. A typical value, however, for $\frac{N}{2\upsilon}$ may be a small as 4 frequency domain symbol widths. In a representative system where the overall bandwidth of the OFDM system is 6 MHz and where N is 256, this provides an acquisition range of only approximately ± 94 KHz or approximately ±3 ppm.

What is needed is a system for OFDM frequency synchronization that can correct for wide offsets that exceed the spacing between training symbols within the frequency domain bursts.

SUMMARY OF THE INVENTION

Systems and methods for wide frequency offset synchronization are provided by virtue of one embodiment of the present invention. A synchronization data sequence is encoded onto a series of OFDM frequency domain bursts as interburst phase differences between training symbols included within the successive bursts. The interburst phase differences may also encode system configuration information. This technique may be used in conjunction with other synchronization techniques to greatly extend the frequency acquisition range achievable with low cost analog components.

A first aspect of the present invention provides a method for synchronizing a second node to a first node in an OFDM communication system. The method includes: at the second node, receiving a series of frequency domain bursts from the first node where the frequency domain bursts includes training symbols, measuring interburst phase differences for the training symbols, and determining a wide frequency offset based on misalignment of a sequence of the interburst phase differences relative to a known sequence.

A second aspect of the present invention also provides a method of synchronizing a second node to a first node in an OFDM communication system. The method includes: developing at the first node, a series of frequency domain bursts, where frequency

domain bursts include training symbols at a predetermined sequence of positions within the bursts, and including synchronization information in the frequency domain bursts encoded as a series of interburst phase differences for successive training symbol positions of the sequence, and transmitting the frequency domain bursts to the second node.

Further understanding of the nature and advantages of the invention herein may be realized by reference to the remaining portions of the specification and the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 depicts a point to point communication system suitable for implementing one embodiment of the present invention.

FIG. 2 depicts time domain structure of an OFDM burst as exploited by one embodiment of the present invention.

FIG. 3 depicts frequency domain structure of an OFDM burst as exploited by one embodiment of the present invention.

FIG. 4 is a flowchart describing steps of synchronization according to one embodiment of the present invention.

FIG. 5 depicts a receiver according to one embodiment of the present invention.

FIG. 6 depicts a transmitter according to one embodiment of the present invention.

FIG. 7 is a flowchart describing steps of determining wide frequency offset according to one embodiment of the present invention.

DESCRIPTION OF SPECIFIC EMBODIMENTS

FIG. 1 depicts a point to point OFDM communication system 100 suitable for implementing one embodiment of the present invention. The present invention is, however, not limited in application to point to point communication systems and may also be used in, e.g., point to multipoint communications systems, broadcast systems, peer to peer systems, etc. System 100 includes a first node 102 and a second node 104. First node 102 includes a transmitter 106 and a receiver 108. Transmitter 106 and receiver 108 share use of an antenna 110 by employing a diplexer 112. Diplexer 112 is employed in FDD (frequency division duplexing) where transmitter 106 and receiver 108 can operate simultaneously but using different frequencies. The present invention also applies to TDD (time division duplexing) systems where transmitter 106 and receiver 108 employ the same frequency but at different times. Diplexer 112 is then unnecessary. A reference oscillator 114 provides a frequency standard to both transmitter 106 and receiver 108.

Second node 104 includes a transmitter 116 and a receiver 118. Transmitter 116 and receiver 118 share use of an antenna 120 by employing a diplexer 122. Instead of employing its own reference oscillator, second node 104 synchronizes its operation frequency to the signal received from first node 102. Receiver 118 synchronizes to its

received signal and generates a synchronization signal to control the operation frequency of transmitter 116.

The frequency synchronization process described herein takes advantage of both time domain and frequency domain structure of OFDM bursts transmitted from first node 102 to second node 104. FIG. 2 depicts a time domain structure 200 of an OFDM burst as exploited by one embodiment of the present invention. Each burst includes a segment holding N symbols representing a result of applying the Inverse Fast Fourier Transform (IFFT) to an N symbol frequency domain burst. Furthermore, each burst includes a ν symbol cyclic prefix followed by an L symbol supplemental cyclic prefix. The N symbols of the IFFT result follow the cyclic prefixes. Together, the cyclic prefix and supplemental cyclic prefix replicate the last $\nu + L$ symbols of the N symbol IFFT result. The ν symbol cyclic prefix assures reception of the frequency domain symbols input into the IFFT within orthogonal subchannels even in the face of dispersive channel conditions. The L symbols of the supplemental cyclic prefix are used to facilitate synchronization.

FIG. 3 depicts a portion of an OFDM frequency domain structure 300 exploited for synchronization purposes according to one embodiment of the present invention. The frequency domain structure includes ν blocks, each block including one training symbol 302 and a group of N/ν -1 data symbols. Training symbols 302 have known magnitude values and are used to estimate the response of the channel between first node 102 and second node 104. According to one embodiment of the present invention, training

symbols 302 carry phase information useful to the receiver in establishing synchronization and system configuration.

Frequency offset, as measured in frequency domain symbol widths, may be understood as including an integer portion and a fractional portion. $f_{offset} = f_{\text{int}} + \Delta f_{offset}$ The synchronization process described herein first corrects for the fractional portion of the frequency offset and then corrects for the integer portion.

FIG. 5 depicts internal structure of receiver 118 of second node 104. Signals received via antenna 120 first go to a RF processing block 502 where low noise preamplification and filtering occur. A mixer 504 downconverts the processed RF signal to an intermediate frequency (IF) by mixing with the output of a variable frequency oscillator 506. The output frequency of variable frequency oscillator 506 as set by a frequency control block 508 determines the receive frequency of receiver 118. The IF signal is input into an IF processing block 510 which filters and amplifies at an IF frequency. There may be further downconversion to baseband or downconversion may be inherent in the operation of an analog to digital converter 512 which converts its input signal to a baseband series of complex symbol values. The baseband symbols are input to an FIR filter 514. The output of FIR filter 514 is a series of time domain OFDM bursts.

FIG. 4 is a flowchart describing steps of a frequency synchronization process according to one embodiment of the present invention. At step 402, a fractional frequency offset processing block 516 evaluates a cost function based on the fractional frequency offset. The cost function is evaluated using the following expression:

$$d\ (\delta) = \sum_{k=\delta-L+1}^{\delta} x^{*}(k)x(k+N)$$

where $x(k)$ is a received time domain symbol value within structure 200, and where δ represents the position of the first of the N symbols in each time domain OFDM burst as determined by a timing synchronization process such as the one described in U.S. Patent App. No. 09/245,168. The cost function will repeat every $N + \nu + L$ samples. The fractional frequency offset cost function should be averaged over successive bursts by:

$$\bar{d}(\delta) = \sum_{k=0}^{K} d(\delta + k(N + \nu + L))$$

The fractional frequency offset is then given by:

$$\Delta f_{offset} = \frac{1}{2\pi N} \tan^{-1} \frac{\operatorname{Im} \bar{d}(\delta_0)}{\operatorname{Re} \bar{d}(\delta_0)}$$

where $\delta_0 = \arg\min_{\delta} \bar{d}(\delta)$

At step 404, frequency control block 508 adjusts the output frequency of variable frequency oscillator 506 to correct the fractional frequency offset determined in step 402. An integer offset may however remain.

The integer offset is determined by computing a correlation between frequency domain symbol values of successive bursts that occupy positions reserved for training symbols. The magnitude of the correlation signal is used to determine small integer offset, i.e., a component of the integer offset that is less than the spacing between training symbols in structure 300. Phase information encoded onto the training symbols is used to determine wide frequency offset, i.e., how many groups of N/ν symbols are in the integer offset.

An FFT block 520 removes the cyclic prefix from successive OFDM time domain bursts output by FIR filter 514 and converts the bursts to the frequency domain. An integer frequency offset processor 518 determines the small and large integer offsets based on the frequency domain symbols output by FFT block 520.

The small integer offset is determined by first forming:

$$Y(n) = \sum_{k=0}^{K} X^{*}(n,k)X(n,k+1)$$

where $X(n,k)$ is the the received frequency domain value at frequency domain symbol n and burst k and K is a number of successive bursts over which $Y(n)$ is evaluated, e.g., 40.

A cost function, e_j, is calculated over groups of N/ν frequency domain symbols by

$$e_j = \sum_{n \in J_j} Y(n) \text{ where e.g,. } N/\nu = 8 \text{ and } j \in [-4,3]$$

where J_j is the set of ν frequency indices corresponding to the training symbol positions, and equally spaced by N/ν.

$$J_j = \left[j \ j + \frac{N}{\upsilon} \cdots \right]$$

Small integer offset is determined based on a magnitude of a cost function determined by correlating successive pairs of bursts.

$$f_{small} = \arg\max_j \left| e_j \right|^2$$

The determination of large frequency offset is dependent on synchronization information encoded in the phase relationships between training symbols. There are two sets of training symbols A and B that are used in alternate bursts. Between each training

symbol of burst A and the corresponding training symbol of group B, there is a phase difference $\Delta\phi$ or ($D_0(n)$). Alignment to a sequence derived from the predefined sequence of D_0 values is determined at the receiver end to estimate large integer frequency offset. In addition to the synchronization sequence, D_0 values may also encode system configuration information.

Fig. 6 depicts elements of transmitter 106 according to one embodiment of the present invention. A physical layer processor 702 coordinates overall transmitter operation, defines encoding and modulation parameters, and arranges for their transmission. Data to be transmitted is input to a Reed-Solomon encoder 704. Data output by Reed-Solomon encoder 704 is in the form of Reed-Solomon codewords. Each codeword includes 2*t parity bytes where t is defined by a configuration signal from physical layer control processor 702.

Reed-Solomon codewords are forwarded to a byte interleaver 706. Byte interleaver 706 reorders the encoded bytes to improve resistance to burst channel impairments. The time span over which byte interleaver 706 reorders bytes is known as the interleaver depth and is controlled by an interleaver depth signal generated by physical layer control processor 702.

A convolutional encoder 708 applies a convolutional code. The degree of redundancy introduced by convolutional encoder 708 may be varied by periodic deletions of its output bits. Variation in the frequency of deletions implements a variation in the convolutional encoder rate, i.e., the ratio of input bits to output bits. The rate is controlled by a signal from physical layer control processor 702.

The output of convolutional encoder 708 is then input into a symbol mapper 710. Symbol mapper 710 maps bits to symbols in accordance with a currently defined symbol constellation. Symbol mapper 710 may employ a variety of constellations. The currently employed constellation is determined by a constellation size control signal generated by physical layer control processor 702. The output of symbol mapper 710 then consists of a stream of data symbols for inclusion within frequency domain OFDM bursts.

Physical layer control processor 702 also outputs system configuration information to be encoded onto training symbols. In one embodiment, a single byte indicates a current constellation size, convolutional code rate, interleaver depth, and number of Reed-Solomon parity bytes. The mapping between possible values of these parameters and byte values within a single system configuration byte is presented in the following table:

Parameter	Possible Values	Bit Mapping
Constellation Size	4	00XX XXXX
	16	01XX XXXX
	64	10XX XXXX
	256	11XX XXXX
Code Rate	½	XX00 XXXX
	2/3	XX01 XXXX
	5/6	XX10 XXXX
	7/8	XX11 XXXX
Interleaver Depth	4	XXXX 000X
	6	XXXX 001X
	9	XXXX 010X
	12	XXXX 011X
	18	XXXX 100X
	24	XXXX 101X
	28	XXXX 110X
	36	XXXX 111X
RS Parity	14	XXXX XXX0
	20	XXXX XXX1

There are two sets of QPSK symbols that are used for the training symbols. These two sets of training symbols, set A and set B, are developed by training symbol symbol formation block 714 and sent in alternating OFDM bursts. Set A is selected to have a low Peak-to-Mean Power Ratio (PMPR). Set B is a modulated version of set A. The modulation is based on a synchronization sequence and the configuration data.

The synchronization sequence, p, is a binary, maximal length sequence of length ν. This binary sequence defines a set of 0 or 90 degree phase shifts in set A. That is, if $p(k) = 0$, $C(k) = \mathrm{A}(k)$, and if $p(k)=1$, $\mathrm{C}(k)=\mathrm{A}(k)*\exp(j*\pi/2)$.

The data sequence is formed from the 8 bits of configuration data described in system configuration byte. These data bits are differentially encoded to form sequence d, and mapped to 0 or 180 degree phase shifts, and then applied to $C(k)$ to form $B(k)$. Thus, $B(k)=C(k)$ for $0<k<\nu-8$; $B(i+\nu-8)=C(i+\nu-8)$ for $i=0..7, p(i)=0$, and $B(i+\nu-8)=-C(i+\nu-8)$ for $i=0..7, p(i)=1$.

The output of differential coding block 716 consists of sets of training symbols for inclusion within bursts of type A and B. The sets of training symbols are output in an alternating pattern, i.e., bursts k, $k+2$, $k+4$ ... use set A while bursts $k+1$, $k+3$, ... use set B.

A selection block 718 then forms successive bursts of type A and B by combining the frequency domain data symbols output by symbol mapper 710 and the training symbols output by differential coding block 716. In one embodiment, the training symbols are evenly spaced through the burst. Selection block 718 forms the bursts and

outputs successive frequency domain OFDM bursts to an IFFT block 720. IFFT block 720 converts the frequency domain burst to the time domain and affixes cyclic prefixes. A transmitter system 722 converts the baseband digital signal to analog, upconverts the signal to an intermediate frequency (IF), amplifies and otherwise processes the IF signal, upconverts the IF signal to a radio frequency (RF), amplifies and otherwise processes the RF signal, and transmits the RF signal via an antenna 724.

There is a synchronization sequence of interspersed phase differences for the training symbols described by the expression:

$$D_0 = Z_A^*(n)Z_B(n)\forall n \in 1 \ldots \nu;$$

Sequence alignment is based on the differences between successive D_0 values from training symbol position to training symbol position. To facilitate the determination of the large integer frequency offset, integer frequency offset processor 518 maintains not only the D_0 values but also a series of D_1 values representing these position to position phase differences. The D_1 sequence is derived from the D_0 sequence by:

$$D_1(n) = D_0(n)D_0^*(n+1)\forall n \in 1 \ldots \nu,$$

where $D_0(1) = D_0(\nu)$

A sequence of D_2 values is also maintained as follows:

$$D_2(n) = |\operatorname{Re}(D_1(n))| + i|\operatorname{Im}(D_1(n))|\forall n \in 1 \ldots \nu$$

Estimates of the D_0, D_1, D_2 sequences are formed by integer frequency offset processor 518 over K bursts using the received training tone values T_1, Fig. 7 is a flowchart

describing steps of determining large integer frequency offset according to one embodiment of the present invention. At step 802, the D_0 values are estimated for each burst k by:

$$\hat{D}_0(n,k) = X^*(n,k)X(n,k+1)\ \forall n \in 1 \ldots \nu, \text{ and } \forall k$$

At step 804, the D_1 values are estimated by:

$$\hat{D}_1(n) = \frac{1}{K-1}\sum_{k=1}^{K-1} \hat{D}_0(n,k)\,\hat{D}_0(n+1,k)$$

where $\hat{D}_0(1) = \hat{D}_0(\nu)$

As can be seen, the D_1 values are smoothed over bursts.

The D_2 values are then estimated based on:

$$\hat{D}_2(n) = \left|\mathrm{Re}(\hat{D}_1(n)\right| + i\left|\mathrm{Im}(\hat{D}_1(n))\right| \forall n \in 1 \ldots \nu,$$

The large integer frequency offset is determined by calculating costs for each possible alignment of the received estimate D_2 values to the D_2 values derived from the known D_0 sequence. The cost function is:

$$dl(r) = \sum_{M=0}^{\upsilon-1} \hat{D}_2(M+r)\,D_2(M)$$

where $r = [-\upsilon/2 \ldots\ldots \upsilon/2]$

At step 806, the large integer offset is determined based on the maximum value of $dl(r)$ as follows:

$$dl_{\max} = \arg\max_{r} dl(r)$$

$$f_{l\arg e} = \frac{N}{\upsilon} dl_{\max}$$

At step 808, system configuration data is retrieved from the last 8 training symbols. First, the order of the alternating training symbols sets A and B must be determined. This order can be determined by finding:

$$\sum_{n \in J_{config}} \mathrm{Im}(\hat{D}_1(n = dl_{\max}))\, \mathrm{Im}(D_1(n)) > 0$$

where J_{config} is the set of training symbols carrying configuration information. If this inequality is true than A precedes B while if the inequality is not true then B precedes A. After the order of the alternating training symbol sets is determined, the values of the bits of the system configuration byte can then be determined.

For each of the positions in J_{config}, the configuration data can be found by comparing the phase of D_l to the known synchronization sequence, $C(K)$. If $D_l(K)$ is within 90 degrees of $C(K)$, then the configuration data for the corresponding symbol is 0, otherwise the data is 1.

The total integer frequency offset is then the total of the large integer and small integer offsets. Referring again to Fig. 4, at step 412, frequency control block 508 adjusts the operating frequency of variable frequency oscillator 506 to correct for both the large and small integer offsets as determined by integer frequency offset processing block 518. The receive frequency of receiver 118 is then aligned to the transmit frequency of transmitter 106. The output of variable frequency oscillator 506 can then serve as a

frequency synchronization signal to transmitter 116 so that transmitter 116's transmission frequency will then be locked to the transmission frequency of transmitter 106. A signal processing block 522 performs further signal processing on the frequency domain training and data symbols to recover transmitted data. This processing includes estimation of the channel response and correction of the received data symbols for the estimated channel response.

It is understood that the examples and embodiments described herein are for illustrative purposes and that various modifications or changes in light thereof will be suggested to persons skilled in the art and are to be included within the spirit and purview of this application and scope of the appended claims and their full scope of equivalents. For example, the present invention may be applied to wired systems rather than wireless systems. Also, it will be appreciated that the present invention may be applied to receiver systems that incorporate input from multiple antennas. All publications, patents and patent applications cited herein are hereby incorporated by reference.